



EV372454211

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/875,501
Filing Date June 4, 2001
Inventor Klaus F. Schuegraf, et al.
Assignee Micron Technology, Inc.
Group Art Unit 2815
Examiner E. Ortiz
Attorney's Docket No. MI22-1741
Title: Methods for Forming Wordlines, Transistor Gates, and Conductive Interconnects,
and Wordline, Transistor Gate, and Conductive Interconnect


SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

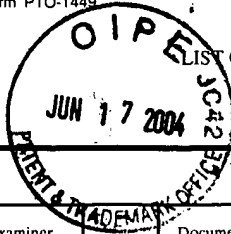
The Examiner's attention is directed to the references which are listed on the attached Form PTO-1449, a copy of which is attached. No admission is made regarding whether all the submitted references are prior art.

Citation of these references is respectfully requested.

Respectfully submitted,

Dated: 6-17-04

By: 
D. Brent Kenady
Reg. No. 40,045

Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. MI22-1741		SERIAL NO. 09/875,501	
 LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Klaus Schuegraf, et al.			
				FILING DATE June 4, 2001		GROUP 2815	
U.S. PATENT DOCUMENTS							
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
AA	5,731,239	03/24/98	Wong et al.				
AB	5,837,601	11/17/98	Matsumoto				
AC	5,766,994	06/16/98	Tseng				
AD	5,851,891	12/22/98	Dawson et al.				
AE							
AF							
AG							
AH							
AI							
AJ							
AK							
AL							
FOREIGN PATENT DOCUMENTS							
	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
AM							
AN							
AO							
AP							
AQ							
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
AR							
AS							
AT							
EXAMINER				DATE CONSIDERED			
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							